

(19)日本国特許庁 (J P)

(12) 公開特許公報 (A)

(11)特許出願公開番号

特開平7-311708

(43) 公開日 平成7年(1995)11月28日

(51) Int.Cl. *

識別記号 庁内整理番号
523 C 7608-5B

FIG

技术表示简所

G 11 C 17/ 00

510 Z

審査請求 未請求 請求項の数4 OL (全 11 頁)

〈21〉出願番号

特願平6-103522

(71) 出願人 391051588

富士フィルムマイクロデバイス株式会社
宮城県黒川郡大和町松坂平1丁目6番地

(22) 出題日

平成6年(1994)5月18日

(71) 出願人 00000520

富士写真フィルム株式会社
神奈川県南足柄市中沼210番地

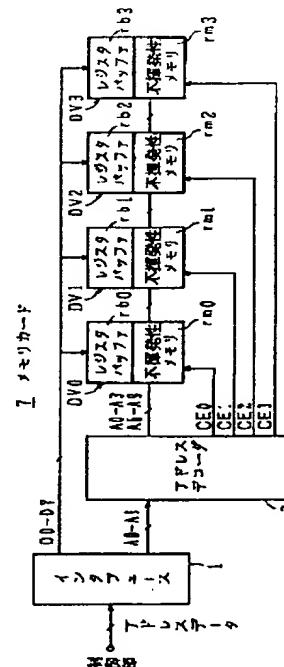
(72) 発明者 庭野 浩之

宮城県黒川郡大和町松坂平1丁目6番地
富士フィルムマイクロデバイス株式会社内

(74) 代理人 弁理士 高橋 敏四郎 (外1名)

(54) [発明の名称] メモリカード

(57) · · · · · · ·



(2)

FUSA 005754

(4)

FUSA 005756

(5)

FUSA 005757

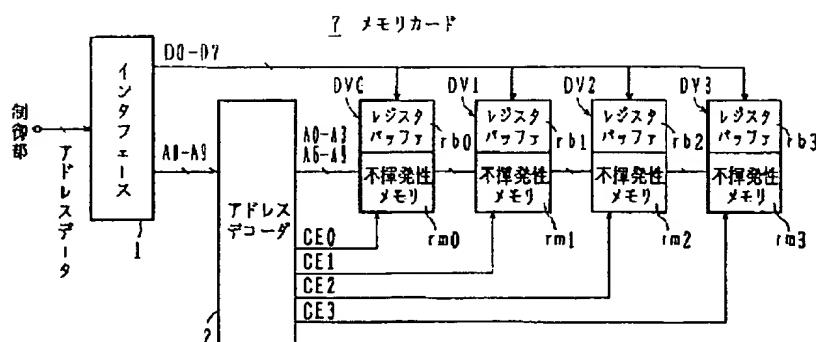
(6)

FUSA 005758

(7)

FUSA 005759

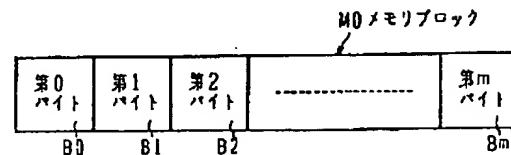
実施例 1



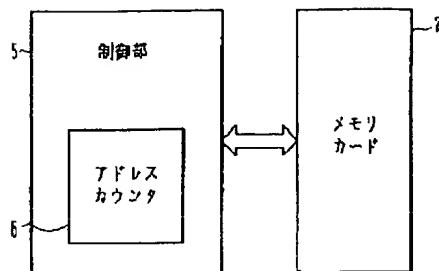
アドレス信号

不揮発性メモリブロック (A0~A3)

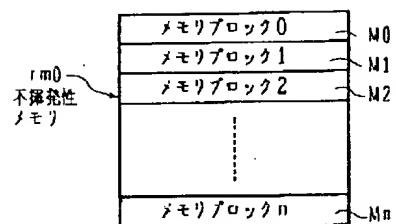
A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
不揮発性メモリブロック アドレス (M0-M15)	CE0-CE3 デコード	パッファメモリ転送 アドレス (B0-B15)							



全体構成

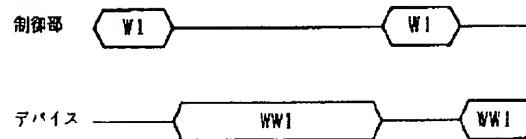
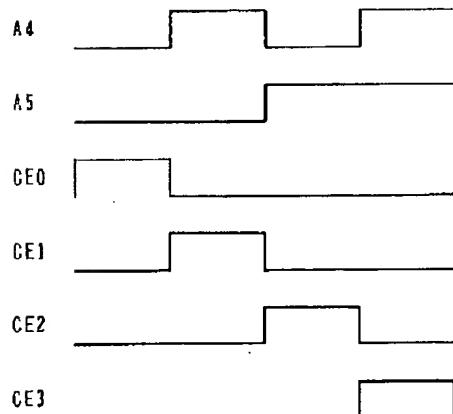


不揮発性メモリ (A6~A9)

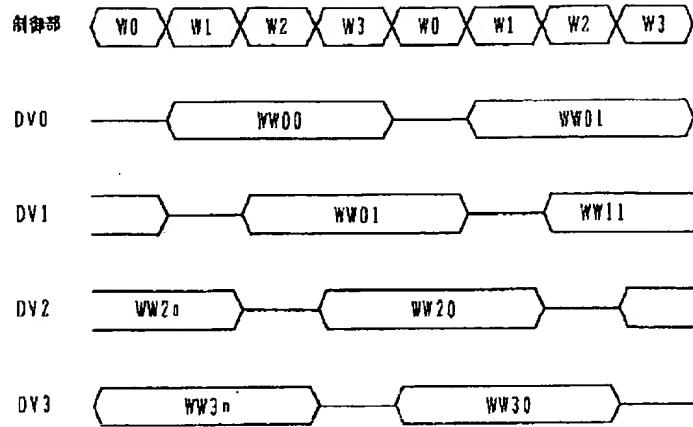


従来技術

チップアイネーブル信号

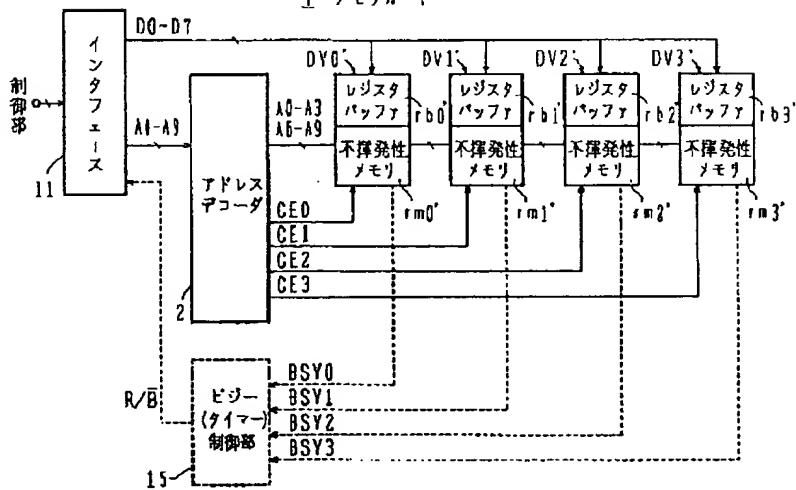


実施例1のタイミングチャート

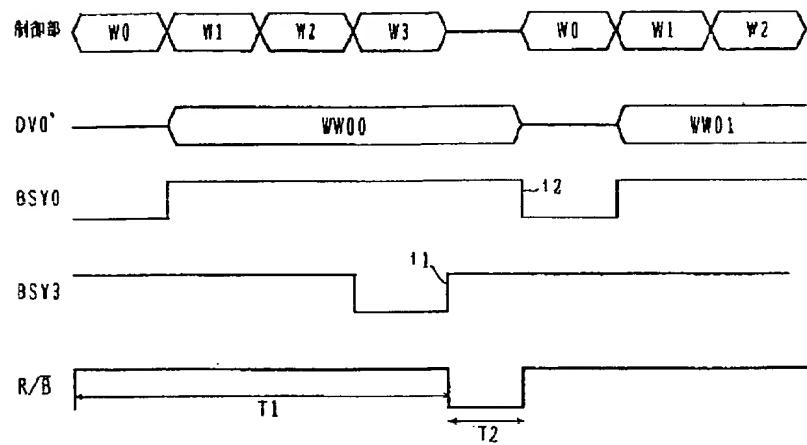


実施例2

7 メモリカード



実施例2のタイミングチャート



JAPANESE LAID-OPEN PATENT APPLICATION

{PRIVATE }

H7-311708 (1995)

(19) Japan Patent Office (JP)

(11) Publication No. H7-311708

(12) Published Unexamined Patent Application (A) (43) Publication Date November 28, 1995

(51) Int. Cl.⁶ Identification Code In-House Reference. No. FI

G 06 F 12/06 523 C 7608-5B

G 11 C 17/00 510 Z

(21) Application No.

PA H6-103522

(22) Date of Filing

May 18, 1994 (Heisei 6)

(71) Applicant

391051588

Fuji Film Micro Device K.K.

1-6 Matsuzakadaira, Yamato-Cho

Kurokawa-Gun, Miyagi-Ken

(71) Applicant

000005201

Fuji Photo Film Co., Ltd.

210 Nakanuma, Minami Ashigara-shi

Kanagawa-Ken

(72) Inventor

Hiroyuki NIWANO

c/o Fuji Film Micro Device K.K.

1-6 Matsuzakadaira, Yamato-Cho

Kurokawa-Gun, Miyagi-Ken

{PAGE }

(74) Agent

Keishiro TAKAHASHI, Attorney

(and 1 other)

(54) Title of the Invention

MEMORY CARD

(57) Abstract

Purpose:

To provide a nonvolatile memory card having the ability to access a large capacity of data in a short time.

Construction:

This memory card stores write data D0 - D7 according to externally supplied successive addresses A0 - A9, and has an address decoder 2 which generates enable signals CE0 - CE3, memory block select signals A6 - A9, and in-block address signals A0 - A3 according to the externally supplied addresses A0 - A9, and a plurality of memory devices DV0 - DV3 which include buffers rb0 - rb3 which temporarily store the write data in addresses indicated by the in-block address signals and nonvolatile memories rm0 - rm3 which have a plurality of memory blocks capable of storing a specific capacity of data. The write data are stored in one of the buffers of the a plurality of memory devices DV0 - DV3 selected in order according to the enable signals, and the memory devices transfer the specific capacity of data stored in the buffers to the memory blocks that correspond to the memory block select signals.

Selected Drawing

Embodiment 1

{PAGE }

7 Memory Card

Controller, Address data

1 Interface

2 Address Decoder

DV0

Rb0 Register Buffer

Rm0 Nonvolatile memory

DV1

Rb1 Register Buffer

Rm1 Nonvolatile memory

DV2

Rb2 Register Buffer

Rm2 Nonvolatile memory

DV3

Rb3 Register Buffer

Rm3 Nonvolatile memory

Claims

Claim 1

A memory card which stores write data according to externally supplied successive addresses A0 - A9 and write data D0 - D7, and

a memory card comprises an address decoder 2 which generates enable signals CE0 - CE3, memory block select signals A6 - A9, and in-block address signals A0 - A3 according to the externally supplied addresses A0 - A9; and

a plurality of memory devices DV0 - DV3 which include buffers rb0 - rb3 which temporarily store the write data in addresses indicated by the in-block address signals and nonvolatile memories rm0 - rm3 which have a plurality of memory blocks capable of storing a specific capacity of data; and, the write data are stored in one of the buffers of the a plurality of memory devices selected in order according to the enable signals, and the memory devices transfer the specific capacity of data stored in the buffers to the memory blocks that correspond to the memory block select signals.

Claim 2

In addition, a memory card according to Claim 1, comprising a busy signal generation means which generates a busy signal when data is being written into the memory, and a busy control means (15) which generates a ready signal (R/-B) which indicates a state where writing to the memory card is possible according to a plurality of the busy signals (BSY0 - BSY3) generated corresponding to a plurality of the memory devices.

Claim 3

A memory card which reads stored data according to externally supplied successive addresses A0 - A9, and

a memory card, comprising

an address decoder 2 which generates enable signals CE0 - CE3, memory block select signals A6 -

A9, and in-block address signals A0 - A3 according to the externally supplied addresses A0 - A9; and

nonvolatile memories rm0 - rm3 which have a plurality of memory blocks capable of storing a specific capacity of data; and,

the address data is read according to the in-block address signal from the memory block according to the memory block selective signal with one of the memory devices from among the plurality of memory devices selected in order according to the enable signals.

Claim 4

In addition, a memory card according to Claim 3, comprising a busy signal generation means which generates a busy signal when data is being read from the memory, and a busy control means (15) which generates a ready signal (R-/B) which indicates a state where reading from the memory card is possible according to a plurality of the busy signals (BSY0 - BSY3) generated corresponding to a plurality of the memory devices.

Detailed Description of the Invention

0001

Industrial Application

The present invention relates to a memory card and especially relates to a memory card which stores data to internally equipped nonvolatile memory.

0002

Description of the Prior Art

A memory card is used when file data or so forth is stored on a personal computer or when the

{PAGE }

image data generated by an electronic camera or so forth is stored. A conventional memory card is equipped with internal SRAM and it stores to that SRAM externally supplied data and so forth.

0003

In order to maintain storage of the data in the SRAM, a backup power supply circuit is required. This is not desirable as equipping a power supply circuit internally into a memory card leads to size enlargement and a higher price for the memory card.

0004

Therefore, memory cards using nonvolatile memory that do not require a backup power supply have been spreading in recent years. Although nonvolatile memory, such as an EEPROM, does not require a backup power supply, it has the fault that the writing speed to a memory device is slow. In order to cover this fault, memory devices (for example, Toshiba 16Mb NAND type EEPROM, INTEL 16Mb FLASH, ATMEL 4Mb EEPROM, or so forth) which equip a register buffer for temporarily storing the externally supplied data together with the nonvolatile memory are being produced commercially.

0005

This device stores the data supplied from an external controller first to the register buffer. Since the register buffer is volatile memory, the writing speed is quick after the same manner as SRAM and data transfer from a controller to the register buffer can be completed in a short time.

0006

After a specific capacity of data is stored in the register buffer, next the data transfer from the register buffer to nonvolatile memory can be performed. Since the program (writing) to nonvolatile memory requires time, the data transfer rate from a register buffer to nonvolatile memory becomes

{PAGE }

slow.

0007

Fig. 10 shows the timing chart at the time of writing data to the device of a nonvolatile memory which has a register buffer. A controller supplies write data to the device. The data sent from the controller are stored in the volatile register buffer in the device (write cycle W1), and the transfer time is completed in a short time.

0008

After a specific capacity of data is stored in a register buffer, the device will transfer data to nonvolatile memory from a register buffer by the write cycle WW1 thereby performing writing (program). Since the program to nonvolatile memory can be performed only by a low speed, the write cycle WW1 requires a long time as compared with the write cycle W1.

0009

Although the controller has the ability to perform the next processing at the time it originally completed the data writing of the write cycle W1, the data stored in the register buffer cannot perform data writing from a controller to a register buffer while writing (WW1) is being performed to nonvolatile memory.

0010

Accordingly, after the controller completes data writing (W1) to the register buffer within a device and after further waiting for the completion of the data writing (WW1) to nonvolatile memory from the register buffer within a device, it resumes the data writing (WW1) to a device (register buffer).

0011

{PAGE }

FUSA 005770

Problem Solved by the Invention

A nonvolatile memory device which has a register buffer can successively receive only a predetermined amount of data at once from an external controller. The predetermined amount of data is equivalent to the storage capacitance of the register buffer. Although the controller does not have a problem in collecting and transferring the data of the amount within the register buffer capacity to a device, when an amount of data that exceeds that is successively transferred, it must transfer the data over a period of time by dividing it into multiple transfers.

0012

The controller is unable to transfer subsequent data immediately after transferring the data of the register buffer capacity to a device; it must wait until the device is completely finished with the data transfer to the nonvolatile memory from the register buffer. Therefore, storing mass data into a device requires waiting for a long time.

0013

The purpose of the present invention is to provide a memory card which can perform writing or reading of mass data in a short time.

0014

Means to Solve the Problem

The memory card of the present invention stores write data according to externally supplied successive addresses A0 - A9 and write data D0 - D7, and the memory card comprises an address decoder 2 which generates enable signals CE0 - CE3, memory block select signals A6 - A9, and in-block address signals A0 - A3 according to the externally supplied addresses A0 - A9; and a

plurality of memory devices DV0 - DV3 which include buffers rb0 - rb3 which temporarily store the write data in addresses indicated by the in-block address signals and nonvolatile memories rm0 - rm3 which have a plurality of memory blocks capable of storing a specific capacity of data; and, the write data are stored in one of the buffers of the a plurality of memory devices selected in order according to the enable signals, and the memory devices transfer the specific capacity of data stored in the buffers to the memory blocks that correspond to the memory block select signals.

0015

Furthermore, the memory card of the present invention which reads stored data according to externally supplied successive addresses A0 - A9, and the memory card comprising an address decoder 2 which generates enable signals CE0 - CE3, memory block select signals A6 - A9, and in-block address signals A0 - A3 according to the externally supplied addresses A0 - A9; and nonvolatile memories rm0 - rm3 which have a plurality of memory blocks capable of storing a specific capacity of data; and, the address data is read according to the in-block address signal from the memory block according to the memory block selective signal with one of the memory devices from among the plurality of memory devices selected in order according to the enable signals.

0016

Operation

Successive address spaces which follow a plurality of memory devices (DV0 - DV3) can be specified without performing complicated address conversion by generating three signals, an enable signal (CE0 - CE3), a memory-block selection signal (A6 - A9), and an in-block address signal (A0 - A3), based on the externally supplied successive addresses (A0 - A9). Since a buffer can input (write) or output (read) data at high speed, the memory card can perform writing or reading of external data without waiting for the data transfer between the buffer and memory to be completed.

0017

Embodiment

Fig. 2 is a block diagram showing the entire composition of when the controller 5 accesses data in the memory card 7 according to the Embodiment of the present invention. The controller 5 has the ability to write mass image data or so forth to a memory card as well as read from it.

0018

The controller 5 has an address counter 6, and performs writing or reading of successive data of image data or so forth to the successive logical address fields. The address counter 6 counts the 10-bit address signals A0 - A9. By sending out the address signal A0 - A9 set up by the address counter 6 to the memory card 7, the controller 5 writes image data or so forth to the memory card 7, or reads such from it. The start address at which the address counter 6 starts a count is specified by the controller 5.

0019

Fig. 1 is the block diagram showing the composition of the memory card 7 according to the Embodiment of the present invention. Writing or reading of the data from the controller is performed with the memory card 7. Although the operation at the time of writing data is hereafter described as the example, reading can be performed similarly.

0020

When data are written to the memory card 7 from an external controller, an address signal and a data signal are input into the interface 1 within the memory card 7. The interface 1 converts the address signals and data signals which are supplied from the controller into the address signals A0 - A9 and the data signals D0 - D7 having predetermined forms.

0021

The address signals A0 - A9 are the signals for specifying the address space indicated by 10 bits within the memory card 7. The data signals D0 - D7 are data, such as 1 byte (8 bits) of image data, that are desired to be written into the memory card 7. Since the memory card 7 has the ability to store 1 byte of data to one address space, the interface 1 groups the address signals A0 - A9 and the data signals D0 - D7 before outputting.

0022

The memory card 7 has four devices DV0, DV1, DV2, and DV3. The number of devices does not need to be four and they can be set to the optimal number according to the program time in a device. Details regarding the program time will be described hereafter.

0023

The four devices DV0 - DV3 all have the same composition. The device DV0 has the register buffer rb0 and nonvolatile memory rm0 and can write data D0 - D7 to the register buffer address rb0 as indicated by the address signals A0 - A3 and A6 - A9 only when the chip enable signal CE0 is supplied. It cannot write when the chip enable signal CE0 is not supplied.

0024

The data D0 - D7 supplied to the device DV0 are first stored in the register buffer rb0 within the device DV0 according to address signals A0 - A3. If the addresses A0 - A3 are counted one by one in turn, a total of 16 bytes of data will be stored in the register buffer rb0. If 16 bytes of data are stored in the register buffer rb0, a trigger signal will occur within a device DV0, and 16 bytes of data transfer will begin from the register buffer rb0 to nonvolatile memory rm0. The transfer rate to nonvolatile memory rm0 is a low speed.

0025

In addition, the signal for starting data transfer may also be supplied from outside the device DV0 instead of having the device DV0 itself generate the trigger signal which directs the start of data transfer. In this case, the writing data units are not limited to only 16 bytes but should be within the capacity of the register buffer.

0026

Here, the device DV0 makes the unit for 16 bytes which performs data transfer from the register buffer rb0 to nonvolatile memory rm0 into 1 block. The 1 block is not limited to only 16 bytes but depends on the capacity of the register buffer and can be changed. For example, 512 bytes or 1K byte or so forth is sufficient. The destination address that was transferred to nonvolatile memory rm0 from the register buffer rb0 is determined by the address signals A6 - A9. The address signals A6 - A9 specify one block from among a plurality of blocks which it had stored in nonvolatile memory rm0.

0027

Fig. 4 is a schematic diagram showing the composition of the nonvolatile memory rm0 in the device DV0 shown in Fig. 1. In addition, the nonvolatile memories rm1 - rm3 in other devices DV1 - DV3 are comprised of the same composition. The nonvolatile memory rm0 is divided into n numbers of memory blocks M0 - Mn. Data is transferred from the register buffer to any one of the memory blocks M0 - Mn for (n+1). Although the memory block to which a transfer is performed is determined by the 4-bit address signals A6 - A9, when using the 4-bit address signal A6 - A9 in this manner in the present Embodiment, it is set to n<=15, and nonvolatile memory rm0 will consist of 16 or fewer memory blocks. Below, the number of memory blocks is made to 16.

0028

For example, if the address signals A6 - A9 are "0000", memory block 0 (M0) will be specified, and

{PAGE }

if the address signals A6 - A9 are "0001", memory block 1 (M1) will be specified.

0029

Fig. 5 is a schematic diagram showing the composition of memory block M0 shown in Fig. 4. In addition, other memory blocks M1 - Mn within the nonvolatile memory have the same composition. Memory block M0 has the memory area B0 - Bm of $(m+1)$ byte. Although the memory area in which data are stored is determined by the address signals A0 - A3, when they are determined by 4-bit address signals A0 - A3 as in the present Embodiment, it is set to $m = 15$, and the memory block will have 16 bytes of memory area.

0030

For example, if address signals A0 - A3 are "0000", the 0th byte (B0) will be specified, and if address signals A0 - A3 are "0001", the 1st byte (B1) will be specified.

0031

In Fig. 1, the address signals A0 - A9 output from the interface 1 are supplied to the address decoder 2. The address decoder 2 outputs to four devices DV0 - DV3 a total of 8 bits of the address signals A0 - A3 and A6 - A9 supplied from the interface 1, and the address signals A4 and A5 are converted into four chip enable signals CE0 - CE4. The converted chip enable signals CE0 - CE3 are supplied to the devices DV0 - DV3 to which they respectfully correspond, and the operation of each devices DV0 - DV3 is permitted.

0032

Fig. 6 is a signal wave form showing a method in which the address decoder 2 shown in Fig. 1 converts the address signals A4 and A5 to the chip enable signals CE0 - CE3. The address decoder 2 receives the address signals A4 and A5 then outputs the chip enable signals CE0 - CE3. At the

{PAGE }

FUSA 005776

time when the address signals $A_5 = "0"$ and $A_4 = "0"$, only the chip enable signal CE_0 is set to "1" and the remaining chip enable signals $CE_1 - CE_3$ are altogether set to "0." The chip enable signal CE_1 is set to "1" at the time when the address signals $A_5 = "0"$ and $A_4 = "1"$, the chip enable signal CE_2 is set to "1" at the time when the address signals $A_5 = "1"$ and $A_4 = "0"$, and the chip enable signal CE_3 is set to "1" at the time when the address signals $A_5 = "1"$ and $A_4 = "1."$ That is, according to the address signals A_4 and A_5 , any one of the four chip enable signals $CE_0 - CE_3$ turns into "1." The chip enable signals $CE_0 - CE_3$ are signals which permit the writing to the register buffers $rb_0 - rb_3$ within the devices $DV_0 - DV_3$ which respectively correspond.

0033

Fig. 3 is drawing for explaining each bit line of the address signals $A_0 - A_9$ that are supplied to the address decoder 2 from the interface 1 shown in Fig. 1. The address signals $A_0 - A_9$ are signals which consist of 10 bits, and increase in order one by one with the writing of data. The lower order 4 bit signals $A_0 - A_3$ specify memory areas $B_0 - B_{15}$ within the block of nonvolatile memory through the register buffer. The bit signal A_4 and A_5 are the signals for generating the chip enable signals $CE_0 - CE_3$ as mentioned above. The higher order 4 bit signals $A_6 - A_9$ specify the blocks $M_0 - M_{15}$ within the nonvolatile memory.

0034

In Fig. 1, an address decoder 2 supplies address signals $A_0 - A_3$ and $A_6 - A_9$ to all the devices $DV_0 - DV_3$ supplying one to each devices $DV_0 - DV_3$ respectively that correspond to the chip enable signals $CE_0 - CE_3$. The interface 1 supplies data signals $D_0 - D_7$ to all the devices $DV_0 - DV_3$.

0035

An example is given below of the operation in which data $D_0 - D_7$ are written to devices $DV_0 - DV_3$ for when the address signals $A_0 - A_9$ supplied to the address decoder 2 begin from "0000000000". Here, the bit order of the address signals assign the bit in the left corner to be the

{PAGE }

highest order bit.

0036

Since the address signals A5 = "0" and A4 = "0" when the address signals A0 - A9 are "0000000000", chip enable signal sets only CE0 to "1" and writing is permitted to only device DV0. The register buffer rb0 of the device DV0 stores data D0 - D7 in the 0th byte of buffer area since the address signals A0 - A3 are "0000".

0037

Next, since the address signals A0 - A9 are incremented, the address signals A0 - A3 are set to "0001", and the following data D0 - D7 are stored in the buffer area of the 1st byte of the register buffer rb0. Hereafter, the data accumulation to the register buffer rb0 is repeated until the address signal increases to "1111", and data are accumulated at all the buffer areas from the 0th byte to the 15th byte. At this time, the address signals A4 - A9 remain "000000" and do not change.

0038

If data are accumulated at all the buffer areas of the register buffer rb0, the trigger signal for to begin transfer from the register buffer rb0 to the nonvolatile memory rm0 will occur within the device DV0. Since the address signals A6 - A9 are "0000", 16 bytes of data of the register buffer rb0 are transferred to memory block 0 (M0) for the nonvolatile memory rm0. Memory block 0 (M0) has 16 bytes of memory area (B0 - B15).

0039

Since the device DV0 uniquely controls the data transfer from the register buffer rb0 to the nonvolatile memory rm0, the controller independently performs the incrementing of the address signals A0 - A9 with the processing of the data transfer which the device DV0 performs.

0040

If address signals A0 - A9 are further incremented from "0000001111", they will become "0000010000." Since the address signal A5 is set to "0" and A4 is set to "1", the chip enable signal sets only CE1 to "1" and the device DV1 will be in a state that enables it to write. The device DV0 to which data accumulation was performed until now becomes write-protected. The register buffer rb1 of the device DV1 stores data D0 - D7 in the buffer area from the 0th byte to the 15th byte according to the increase in address signals A0 - A3. Since the address signals A6 - A9 are "0000" when 16 bytes of data are stored in the register buffer rb1, data transfer is performed from the register buffer rb1 to the memory block 0 (M0) of nonvolatile memory rm1.

0041

Since the address signal A5 = "1" and A4 = "0" with the incrementing of the address signal, the chip enable signal CE2 is set to "1" simultaneously with the start of data transfer. The data D0 - D7 are stored in the buffer area from the 0th byte to the 15th byte in the register buffer rb2 of the device DV2 according to the increase in address signals A0 - A3. If 16 bytes of data are stored in the register buffer rb2, data transfer will be performed from the register buffer rb2 to the memory block 0 (M0) of the nonvolatile memory rm2.

0042

With the incrementing of the address signals being carried out with the start of data transfer, the address signal A5 = "1" and A4 = "1", and only the chip enable signal CE3 is set to "1". The data D0 - D7 are stored in the buffer area from the 0th byte to the 15th byte in the register buffer rb3 of the device DV3 according to the increase in address signals A0 - A3. If 16 bytes of data are stored in the register buffer rb3, data transfer will be performed from the register buffer rb3 to the memory block 0 (M0) of the nonvolatile memory rm3.

0043

If address signals A0 - A9 are further incremented from "0000111111", they will become "0001000000." when incrementing the address signals, since the address signals A5 is set again to "0" and A4 is set again to "0", the chip enable signal sets CE0 to "1" and 16 bytes of data are stored in the register buffer rb0 of the device DV0. Since the address signals A6 - A9 are "0001" when 16 bytes of data are stored in the register buffer rb0, data transfer is performed from the register buffer rb0 to the memory block 1 (M1) of nonvolatile memory rm0.

0044

After data are stored in the memory block 1 (M1) of nonvolatile memory rm0, sequential data are similarly stored in each memory block 1 (M1) of nonvolatile memory rm1, rm2, and rm3 in order. After that, data are stored in order to nonvolatile memory rm0 - rm3 concerning memory block 2 (M2).

0045

In other words, data are stored in turn rm0 (M0) -> rm1 (M0) -> rm2 (M0) -> rm3 (M0) -> rm0 (M1) -> rm1 (M1) -> rm2 (M1) -> rm3 (M1) -> rm0 (M2) -> rm1 (M2) ->... to each memory block M0 - Mn within the nonvolatile memory rm0 - rm3.

0046

Fig. 7 is a timing chart which shows the operation of the controller 5 and the memory card 7 which are shown in Fig. 2. The controller 5 supplies 16 bytes of data to the memory card 7 in the cycle W0 first together with the address signal which begins with 0 for instance. Since 16 bytes of data are the time stored in the register buffer rb0 of the device DV0, the duration of cycle W0 hardly changes the time for the controller 5 to send out data, but it completes within a short time.

0047

After cycle W0 is completed, while a device DV0 starts the data transfer (WW00) from the register buffer rb0 to nonvolatile memory rm0, the controller 5 supplies (W1) the next 16 bytes of data to the memory card 7.

0048

The controller 5 can supply 16 bytes of data to the memory card in the cycle of W0, W1, W2, and W3 continuously without latency time. After the controller 5 completes the data supply of cycle W0, the device DV0 begins the data transfer (WW00) from the register buffer rb0 to the memory block 0 (M0) of the nonvolatile memory rm0. After the data supply of cycle W1 is completed, the device DV1 begins the data transfer (WW10) from the register buffer rb1 to the memory block 0 (M0) of the nonvolatile memory rm1. After the data supply of cycle W2 is completed, the device DV2 starts the data transfer (WW20) from the register buffer rb2 to the memory block 0 (M0) of nonvolatile memory rm2. After the data supply of cycle W3 is completed, the device DV3 starts the data transfer (WW30) from the register buffer rb3 to the memory block 0 (M0) of nonvolatile memory rm3.

0049

Since the data transfer time (WW00) of the device DV0 is equivalent to the program time of the nonvolatile memory rb0, time is necessary. The transfer time (WW00) of the device DV0 in the present Embodiment is exactly that of 3 cycles (W1 – W3) of the data supply of the controller 5. After cycle W3 is completed, the data transfer of the device DV0 is completed and the controller 5 performs data supply to the device DV0 in cycle W0 and continues through to cycle W3.

0050

The memory card 7 can perform data transfer in the order of cycle WW00 -> WW10 -> WW20 ->

{PAGE }

WW30 -> WW01 -> WW11 -> ... -> WW2n -> WW3n to devices DV0 - DV3. Here, cycle WWij means the data transfer which Device DV_i performs from the register buffer rbi to the memory-block j (M_j) of the nonvolatile memory rmi. However, i and j are positive integers.

0051

Since the controller 5 can perform processing independently with each of the devices DV0 - DV3, as long as the data transfer (WWij) of the device DV_i does not overlap in time with the data supply of cycle Wi performed by the controller 5, a problem will not be generated. Moreover, since each device DV0 - DV3 can perform processing independently, there is no problem with the data transfer WWij of devices DV0 - DV3 overlapping in time.

0052

Here, if all the four devices DV0 - DV3 are the same, then the data supply time by the controller 5 is also the same (W0 = W1 = W2 = W3), and the data transfer time of devices DV0-DV3 is also the same (WW00 = WW10 = WW20 = WW30 = WWij).

0053

The data transfer time (WWij) of the devices DV0 - DV3 according to the present Embodiment is equivalent to the time for three cycles (W (i+1) - W (i+3)) of the data supply time of the controller 5 according the following formula.

0054

$$WWij = 3 \times Wi$$

The required minimum number of devices N for providing the shortest write time into the memory card 7 can be derived according to the following formula. However, the number of devices N is an

integer which is rounded down to the nearest decimal point.

0055

$$N = \lceil \frac{WW_{ij}}{W_i} \rceil + 1$$

In this manner, if the data supply time W_i of the controller and the data transfer time WW_{ij} of the device is known beforehand, the optimal number of devices N can be derived. Even if the number of devices were increased to exceed the quantity N , the data write time to the memory card would be the same.

0056

Fig. 8 shows an example of the case of constituting a memory card using a fewer number of devices than the optimal number of devices N . Although the memory card 7 has four devices DV0' - DV3' just as in the Embodiment according to Fig. 1, the data transfer time WW_{ij} is long when compared with the devices DV0 - DV3 of the Embodiment of Fig. 1. Therefore, the number of optimal devices N is set to 5.

0057

In the memory card 7, since the portions having the same reference indicators as the previous Embodiment have the same composition and function, explanations thereof are omitted. The device DV0' outputs a busy signal BSY_0 while performing the data transfer from the register buffer rb_0' to the nonvolatile memory rm_0' . Similarly, the device DV1' - DV3' outputs busy signals BSY_1 - BSY_3 , respectively.

0058

The busy controller 15 generates a ready signal R/B in response to four busy signals BSY_0 - BSY_3 .

Ready signal R-/B is output to an external controller through an interface 11. The controller can perform data supply only when the ready signal R-/B is "1"; and when the ready signal R-/B is "0", data supply cannot be performed.

0059

For example, when there is an attempt to externally supply data to the device DV0' during the time that the busy signal BSY0 is generated, the busy controller 15 can set the ready signal R-/B to "0" and can cause the external data supply to stand by.

0060

Fig. 9 is a timing chart which shows the operation of the memory card shown in Fig. 8. The external controller can successively supply to memory card 16 bytes of data each by the cycles W0, W1, W2, and W3. Moreover, when the data supply of cycle W0 is completed, the device DV0' begins the data transfer (WW00) from register buffer rb0' to the nonvolatile memory rm0'. While the data transfer (WW00) for the device DV0' is being performed, a busy signal BSY0 is set to "1."

0061

In the time t1 when a busy signal BSY3 reverses from "0" to "1", the busy controller 15 reverses the ready signal R-/B from "1" to "0" and interrupts the data supply from the controller. Thereafter, in the time t2 when the busy signal BSY0 reverses from "1" to "0", the ready signal R-/B reverses from "0" to "1" thereby resuming the data supply (W0) from the controller.

0062

In addition, without using busy signals BSY0 - BSY3, a timer can be equipped within the busy controller 15, and the ready signal R-/B can also be generated. In that case, devices DV0 - DV3 do not need to generate busy signals BSY0 - BSY3, and a cycle signal is generated which the busy

controller 15 sets the ready signal R/B to "1" until after time T1 elapses from the start of the cycle WW0, and then sets it to "0" during time T2 after that.

0063

Time T1 is the sum total duration time of cycles W1 and W2 and W3 ($W1 + W2 + W3$), and time T2 is the time of WW0- ($W1 + W2 + W3$). Time T1 and T2 is measured by the timer in the busy controller 15.

0064

As mentioned above, a plurality of devices (for example four pieces) are equipped in the memory card, and based on the successive addresses A0 - A9 supplied from an external controller and by generating the memory area selection signals A0 - A3 which select one byte from within the memory block, the block selection signals A6 - A9 that select one memory block from within the nonvolatile memory, and the chip enable signals CE0 - CE3 that select one device from among the plurality of devices successive data that exceed the capacity of the register buffer within one nonvolatile memory can be written to the memory card without the latency time.

0065

Although the above Embodiment described the operation at the time of performing writing to a memory card, hereafter, the operation for the case of reading is explained. If the address signals A0 - A9 for all 0 are supplied externally, the device DV0 will once read the data D0 - D7 from the memory block 0 (M0) in the nonvolatile memory rm0 through the register buffer rb0, and will output it to an external controller.

0066

Moreover, since the reading time from nonvolatile memory rm0 is completed in a short time, the

{PAGE }

device DV0 may read data D0 - D7 directly from the memory block 0 (M0) in nonvolatile memory rm0 without going through the register buffer rb0, and then output it to the external controller.

0067

After the data are read from the memory block 0 (M0) in the nonvolatile memory rm0, reading of the data is performed from each memory block 0 (M0) in the order of the nonvolatile memory rm1, rm2, and rm3 in the same manner as the time of writing the data according to change of the chip enable signals CE0-CE3.

0068

After that, data reading is similarly performed in the order from the nonvolatile memory rm1, rm2, and rm3 respectively in regard to the subsequent memory blocks according to the increment of the address signals A0 - A9.

0069

In order to generate the ready signal R-B of Fig. 8 at the time of data reading, after device DV0' carries out the data transfer to the register buffer rb0 from the nonvolatile memory rb0', the data stored in register buffer rb0' are output to the external controller. While the device DV0' is carrying out the data transfer from the nonvolatile memory rb0' to the register buffer rb0, the busy signal BSY0 is set to "1."

0070

Although the present invention was described in accordance with the Embodiment given above, the present invention is not limited to these. For example, that various changes, improvements, combinations, or so forth are possible is obvious to one skilled in the art.

{PAGE }

FUSA 005786

0071

Efficacy of the Invention

Since writing or reading can be performed for mass successive data continuously without a time break according to the data-access speed to a buffer according to the memory card of this invention as explained above, writing or reading of data can be performed in a short time.

0072

Moreover, by generating three signals, enable signals (CE0 - CE3), memory block selection signals (A6 - A9), and in-block address signals (A0 - A3) based on the externally supplied consecutive addresses (A0 - A9), even if a plurality of memory devices are used (DV0 - DV3) successive address spaces can be easily specified.

Brief Description of the Drawings

Fig. 1 is a block diagram showing the composition of the memory card according to the Embodiment of the present invention.

Fig. 2 is a block diagram showing the entire composition for when the controller carries out a data access to the memory card according to the Embodiment of the present invention.

Fig. 3 is a chart for explaining each bit line of the address signals A0 - A9 supplied to the address decoder from the interface shown in Fig. 1.

Fig. 4 is a schematic diagram showing the composition of the nonvolatile memory in the device shown in Fig. 1.

Fig. 5 is a schematic diagram showing the composition of memory block shown in Fig. 4.

Fig. 6 is a signal wave form view showing the conversion method from the address signals A4 and A5 to the chip enable signals CE0 - CE3 which the address decoder shown in Fig. 1 performs.

Fig. 7 is a timing chart which shows the operation of the memory card shown in Fig. 6.

Fig. 8 is a block diagram showing the composition of the memory card using a number of devices fewer than the optimal number of devices.

Fig. 9 is a timing chart which shows the operation of the memory card shown in Fig. 8.

Fig. 10 shows a timing chart at the time of writing data to a nonvolatile memory device which has a conventional register buffer.

Description of Notations

1	Interface
2	Address Decoder
5	Controller
6	Address Decoder
7	Memory Card
DV	Device
rb	Register buffer
rm	Nonvolatile memory
M0 - Mn	Memory block
B0 - Bm	Memory area (byte unit)
CE	Chip enable signal
BSY	Busy signal
R-/B	Ready signal
A0 - A9	Address signal
D0 - D7	Data signal

Drawings

Figure 1

Embodiment 1

7 Memory Card (from left to right)

Controller, Address data

1	Interface
2	Address Decoder
DV0	
Rb0	Register Buffer

Rm0 Nonvolatile memory

DV1

Rb1 Register Buffer

Rm1 Nonvolatile memory

DV2

Rb2 Register Buffer

Rm2 Nonvolatile memory

DV3

Rb3 Register Buffer

Rm3 Nonvolatile memory

Figure 2

Entire Composition

5 Controller

6 Address Counter

7 Memory Card

Figure 3

Address Signal

A6 – A9 Nonvolatile memory block address (M0 – M15)

A4 – A5 CE0 – CE3 Decode

A0 – A3 Buffer memory transfer address (B0 – B15)

Figure 4

Nonvolatile Memory (A6 – A9)

M0 Memory block 0

M1 Memory block 1



M2 Memory block 2
Rm0 Nonvolatile Memory
Mn Memory Block n

Figure 5

Nonvolatile Memory Block (A0 – A3)

0th byte B0
1st byte B1
2nd byte B2
M0 Memory Block
Mth byte Bm

Figure 6

Chip Enable Signal

Figure 7

Embodiment 1 Timing Chart

Controller W0 W1 W2 W3 W0 W1 W2 W3
DV0
DV1
DV2
DV3

Figure 8

Embodiment 2

{PAGE }

7 Memory Card

Controller

11 Interface

2 Address Decoder

DV0'

Rb0' Register Buffer

Rm0' Nonvolatile memory

DV1'

Rb1' Register Buffer

Rm1' Nonvolatile memory

DV2'

Rb2' Register Buffer

Rm2' Nonvolatile memory

DV3'

Rb3' Register Buffer

Rm3' Nonvolatile memory

Figure 9

Embodiment 2 Timing Chart

Controller W0 W1 W2 W3 W0 W1 W2

DV0'

BSY0

BSY3

R-/B

Figure 10

Conventional Art

{PAGE }